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METHOD OF SIMULTANEOUSLY IMPLEMENTING DIFFERENTIAL GATE OXIDE THICKNESS USING FLUORINE BEARING IMPURITIES

ABSTRACT OF THE DISCLOSURE

Improved methods for fabricating semiconductor integrated circuit devices, in particular flash EEPROM devices. According to an embodiment, the present invention provides a method of forming a semiconductor device having a gate oxide layer (160) that is thin in some regions, such as the cell region, and thicker in other regions (165), such as the periphery region. The method simultaneously provides a gate oxide layer with two or more thicknesses without the thickness control problems of prior art methods that use contaminant-containing photoresist with an etching step. According to a specific embodiment of the present invention, the gate oxide has a first thickness that is sufficiently thin to provide high driving capability for the semiconductor ROM device, and a second thickness that is sufficiently thick to provide high voltage reliability of the semiconductor ROM device.